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M 2-3

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Texts:

W. Stallings, *Computer Organization and Architecture: Designing for Performance*, Prentice Hall, 2000.

D.A. Patterson and J.L. Hennessy, *Computer Organization & Design: the Hardware/Software Interface*, Morgan Kaufmann Publishers, Inc.

Class Web Page:

<http://www.student.seas.gwu.edu/~kallitec/Architecture/ClassTransparencies/index.html>

Catalog Description:

Enhancing the processor and system performance. Processor architecture and microinstruction execution. Caches. Memory management. Design of the data path and the control unit. Operating system support. Instruction pipelining. Data and control hazards. Microprogramming. Instruction level parallelism. Superscalar RISC processors. Multiprocessors. Introduction to real-time embedded systems.

Objectives:

This is a continuation of ece181 to complete the coverage of topics in Computer Systems Architecture and design. It covers topics such as cache memories, operating system support, memory management, designing hardwired and microprogrammed control units, pipelining concepts and introduction to parallel processing and architectures.

Prerequisites:

ECE 181 (Computer Systems Architecture)

Topics:

1. System buses
2. Memories
3. Caches
4. O/S Support
5. Advanced Input/Output
6. The Control Unit operation
7. Midterm
8. Microprogrammed Control
9. Processor: Datapath and Control
10. Pipelining
11. Superscalar Processors
12. Parallel Processing

Grading:

1. Midterm: 35%
2. Final exam: 45%
3. Homework: 10%
4. Class “interest/participation”: 10%