ECE 201: Microcomputer Systems Architecture

Instructor: *Nikitas A. Alexandridis*

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Office hours: M 1-3 pm

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(others by appointment)

Text: 1) "Computer Systems Architecture: Microprocessor-Based Designs", *N. Alexandridis*, CAPCO, 1999.

2) Notes to be handed out in class

Class Web Page:

http://www.student.seas.gwu.edu/~kallitec/ece201/ece201.htm

ECE 201: Microcomputer Systems Architecture

✍ Catalog Description:

Instruction formats and instruction execution by a computer. Computer systems configurations. RISC, CISC, and superscalar processor architectures. CPU and system performance. Design of bus-based digital computer systems. Bus transfers and control signals. The memory hierarchy (DRAMs, caches, virtual memory). Input/output interfacing and interrupts. Instruction pipelines.

✍ Objectives:

This is an introductory graduate course in computer architecture and design. It adopts a "systems approach" to the design of digital computer systems using state-of-the-art processors. It presents the design and performance of various computer subsystems, and their interconnection and intercommunication using various bus protocols. Subsystems studied include: the main processor, caches, interleaved DRAM memories, input/output, etc. Finally it covers topics in instruction pipelining and superscalar architectures.

✍ Prerequisites:

ECE 181 or an equivalent first course in Computer Organization and a course in Logic Design.

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Topics:

1. Introduction
2. Review material : instruction formats and addressing modes; instruction sequencing; instruction execution cycles.
3. Processor and system performance
4. Computer systems configurations
5. Instruction pipelining
6. Superscalar processors
7. Bus transfers and system interface protocols

8. Midterm

9. I/O interfacing and Industry system buses: Program-driven and interrupt I/O. VME bus, Futurebus, Multibus; sad-/mad- endian bus interfacing and tradeoffs in selecting the system bus.
10. Advanced memory systems design and interfacing: advanced 32- and 64-bit memory designs; DRAM controllers; memory interleaving; advanced DRAM access modes (fast page mode, static column mode, etc.); calculating memory time requirements.
11. Cache memories: system configurations; cache characteristics and organizations; write and cache update policies; hardware/software solutions to cache coherency

13. Memory Management Units (MMUs): logical/virtual addresses and mapping; protected mode memory management; examples of processors with paging and/or segmentation; formats and attributes of page and segment-descriptors; ATC/TLB structures and table-walkthrough mechanisms.
14. Handling external interrupts and protected mode exceptions. Protected mode multitasking.
15. Advances in computer system architectures, multiprocessor systems, embedded systems, etc

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Course textbook:

1) N. Alexandridis, *Computer Systems Architecture: Microprocessor-Based Designs*, CAPCO.
2) Notes to be passed out in class

Useful References:

1. D.A. Patterson and J.L.Hennessy , *Computer Organization and Design: The Hardware/Software Interface*, Morgan Kaufmann Publishers, Inc.
2. W. Stalling, *Computer Organization and Architecture*, Prentice Hall.

Grading:

1) Midterm: 35%
2) Final exam: 45%
3) Homework: 10%
4) Class "interest/participation": 10%